REMARKS

Favorable consideration of the application is respectfully requested. Claims 25-31, 33-38, 40-41, 43, 50-54 and 56, prior to this paper, were pending in the present application. By this paper, claims 25, 26, 30, 34, 35, 37, 38, 40, 41, 50, 51, 53 and 54, are amended.

Specification

The specification, prior to this response, was objected to by the Examiner. Though the phrase "substantially uniform insulative material" is believed to supported by the drawings in the present application, the phrase now reads "insulative material" in the claims as originally filed.

Therefore the Examiner's objection to the specification is overcome.

Claim Rejections - 35 U.S.C. §112

Claims 25-31, 33-38, 40-41, 43, 50-54 and 56, prior to amendment, were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Though the phrase "substantially uniform insulative material" is believed to supported by the drawings in the present application, the phrase now reads "insulative material" in each instance the phrase occurs in claims 25, 30, 34, 37, 38, 50, 53 and 54.

Claims 40-41 and 43, prior to amendment, were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The phrase "oxide filler substantially devoid of other constituents" now reads "oxide filler" in claim 40.

Therefore, by amendment, the rejection of claims 25-31, 33-38, 40-41, 43, 50-54 and 56. under 35 U.S.C. §112, first paragraph, is overcome.

Claims 25-31, 33-38, 40-41, 43, 50-54 and 56, prior to amendment, were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "substantially uniform insulative material" has been amended to read "insulative material" in each instance the phrase occurs in claims 25, 30, 34, 37, 38, 50, 53 and 54.

The phrase "oxide filler substantially devoid of other constituents" has been amended to read "oxide filler" in claim 40.

The phrase "the depth of a border diffusion region" has been amended to read "a depth of a bordering diffusion region" in claims 26, 35, 41 and 51.

Therefore, by amendment, the rejection of claims 25-31, 33-38, 40-41, 43, 50-54 and 56. under 35 U.S.C. §112, second paragraph, is overcome.

Claim Rejections - 35 U.S.C. §102

Claims 50-54 and 56, prior to amendment, were rejected under 35 U.S.C. §102(b) as being anticipated by Sasaki (U.S. Patent No. 4,471,525).

Base claim 50 has been amended to recite:

"...forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench."

The added language further distinguishes the presently claimed invention from Sasaki. Support for the language "said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench" is found in Figs. 1F-1H and 2E-2I, as these drawings demonstrate the absence of bordering diffusion region at the base of the trench. The term "diffusion region" is defined and supported in the specification on page 9, lines 1-3. In fact, the presence of a diffusion region at the base of the isolation trench of the present invention could be detrimental to the intent of the present invention, namely creating isolation between devices of a semiconductor assembly.

Sasaki discloses in Figs. 4D-4H that a p+ diffusion region 50 is formed to border the base trench 47. Sasaki, on column 9, lines 53-55, discloses the formation of a p+ type channel stopper 50 by diffused boron. In fact, in all the embodiments of Sakasi, a p+ channel stopper is formed to border the base of the created trench.

Clearly, Sasaki teaches away from the present claimed invention of forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench, a feature of the presently claimed invention as relied for amendment.

Thus, claim 50, as presently amended, is patentable over the art of record and thus place dependent claims 51-54 and 56 as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 50-54 and 56, under 35 U.S.C. §102(b), as being anticipated by Sasaki, is overcome.

Claim Rejections - 35 U.S.C. §103

Claims 25-31, 33-38, 40-41 and 43, prior to amendment, were rejected under 35 U.S.C. §103(a) as being as being unpatentable over Sasaki in view of Kameyama (U.S. Patent No. 4,472,240).

Base claim 25 has been amended to recite:

> "...forming a second trench into said semiconductor substrate at the bottom of said first trench by using said spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;"

Base claim 34 has been amended to recite:

> "...forming a second trench into said semiconductor substrate at the bottom of said first trench by using said spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;"

Base claim 40 has been amended to recite:

> "...forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said semiconductive spacer as an etching guide, said silicon substrate assembly being devoid of a bordering diffusion region at the base of said second trench;"

language, which further distinguishes the presently claimed invention from Sasaki in view of Kameyama.

Support for the language "...substrate (or substrate assembly) being devoid of a bordering diffusion region at the base of said trench" is found in Figs. 1F-1H and 2E-2I, as these drawings demonstrate the absence of bordering diffusion region at the base of the trench. The term "diffusion region" is defined and supported in the specification on page 9, lines 1-3. In fact, the presence of a diffusion region at the base of the isolation trench of the present invention could be detrimental to the intent of the present invention, namely creating isolation between devices of a semiconductor assembly.

As discussed earlier, Sasaki discloses in Figs. 4D-4H that a p+ diffusion region 50 is formed to border the base trench 47. Sasaki, on column 9, lines 53-55, discloses the formation of a p+ type channel stopper 50 by diffused boron. In fact, in all the embodiments of Sakasi, a p+ channel stopper is formed to border the base of the created trench.

Clearly, Sasaki teaches away from the present claimed invention of forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench, a feature of the presently claimed invention as relied for amendment.

Kameyama discloses the formation of first and second trenches and filling these trenches with an oxide filler. If the Examiner is correct in that Sasaki and Kameyama are combinable, in light of the presently claimed invention this combination would defeat the intent of Sasaki. If a second trench of Kameyama was implemented in any of the embodiments of Kasaki, either the p+ channel stopper formed to border the base of the created trench would be destroyed or the p+ channel stopper would be placed after the second trench is formed and thus resulting in the formation of a p+ channel stopper bordering the base of the created trench. Clearly, either scenario teaches away from the presently claimed invention.

Thus, base claims 25, 34 and 40, as presently amended, are patentable over the art of record and thus place respective dependent claims 26-31, 33, 35-38, 41 and 43 and as patentable over the art of record as well. Therefore, by amendment, the rejection of claims 25-31, 33-38, 40-

41 and 43, under 35 U.S.C. §103(a) as being as being unpatentable over Sasaki in view of Kameyama (U.S. Patent No. 4,472,240), is overcome.

Additional Information

Attached hereto (**Appendix A**) is a marked-up version of the changes made to the claims per Applicant's present response (paper 13).

Also, attached hereto (**Appendix B**) is a clean copy of the current pending 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response (paper 13).

CONCLUSION

Applicant submits that the application is in condition for allowance. Such allowance at an early date is respectfully requested.

To that end, if the Examiner feels that a conference will expedite the prosecution of this case, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

David J. Paul

David J. Paul
Agent for the Applicant
Registration Number 34,692
(208) 368-4515

APPENDIX A

Following is a marked-up version of the changes made per Applicant's present response in paper 13.

In the Claims:

Claims 25, 26, 30, 34, 35, 37, 38, 40, 41, 50, 51, 53 and 54 have been amended as indicated below.

25. (Three Times Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate [assembly] at the bottom of said first trench by using said spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an [a substantially uniform] insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said [substantially uniform] insulative material.

APPENDIX A

26. (Amended) The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times [the] a depth of a bordering diffusion region.

30. (Twice Amended) The process as recited in claim 25, wherein said step of forming said [substantially uniform] insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

34. (Three Times Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate [assembly] at the bottom of said first trench by using said semiconductive spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an [a substantially uniform] insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said [substantially uniform] insulative material;

planarizing said [substantially uniform] insulative material;

wherein said process uses only one mask to form said device isolation.

35. (Amended) The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times [the] a depth of a bordering diffusion region.

37. (Twice Amended) The process as recited in claim 34, wherein said step of forming said [substantially uniform] insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. (Twice Amended) The process as recited in claim 34, wherein said [substantially uniform] insulative material and said single layer dielectric lining are the same type material.

40. (Three Times Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide, said silicon substrate assembly being devoid of a bordering diffusion region at the base of said second trench;

forming an oxide filler [substantially devoid of other constituents] in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

41. (Amended) The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times [the] a depth of a bordering diffusion region.

50. (Three Times Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming an [substantially uniform] insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said [substantially uniform] insulative material.

APPENDIX A

51. (Amended) The process as recited in claim 50, wherein an overall depth of said trench is two times [the] a depth of a bordering diffusion region.

53. (Twice Amended) The process as recited in claim 50, wherein said step of forming an [a substantially uniform] insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. (Twice Amended) The process as recited in claim 50, wherein said [substantially uniform] insulative material and said dielectric lining are the same type material.

APPENDIX B

Following is a copy of the current pending claims 25-31, 33-38, 40-41, 43, 50-54 and 56 per Applicant's present response in paper 13.

25. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate at the bottom of said first trench by using said spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said insulative material.

26. The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

27. The process as recited in claim 25, wherein said spacer is formed from an oxidizable material.

28. The process as recited in claim 25, wherein said spacer is formed of oxide.

29. The process as recited in claim 25, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

30. The process as recited in claim 25, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same type material.

33. The process as recited in claim 25, wherein said process uses only one mask to form said device isolation.

34. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate at the bottom of said first trench by using said semiconductive spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said insulative material;

planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

35. The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

36. The process as recited in claim 34, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

37. The process as recited in claim 34, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. The process as recited in claim 34, wherein said insulative material and said single layer dielectric lining are the same type material.

APPENDIX B

40. A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide, said silicon substrate assembly being devoid of a bordering diffusion region at the base of said second trench;

forming an oxide filler in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

41. The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

43. The process as recited in claim 40, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

50. A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said insulative material.

51. The process as recited in claim 50, wherein an overall depth of said trench is two times a depth of a bordering diffusion region.

52. The process as recited in claim 50, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a trench.

53. The process as recited in claim 50, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. The process as recited in claim 50, wherein said insulative material and said dielectric lining are the same type material.

56. The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.